REMARKS

Claim Objections

Claim 8 was objected to because the claim recited "wherein the" twice, and the examiner requested that one instance be deleted. Applicant was unable to locate a duplicate instance of "wherein the" in claim 8. However, this informality was found in claims 12, 13, and 18 and has been corrected.

Claim 18 was objected to under 37 CFR 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim, and the Examiner indicated that claim 18 claimed the same subject matter as claims 12 and/or 13. Claim 18 has been amended to depend from claim 16.

Double Patenting Rejection

Claims 11, 14, 16 and 17 were provisionally rejected under the judicially created obviousness-type double patenting as being unpatentable over claims 16 and 17 of co-pending U.S. Patent Application Serial No. 09/943,475. Claims 1-21 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of co-pending application no. 09/943,475 in view of *Baltz et al.*

Baltz et al. discloses a method for DMA boot loading for transferring a block of data from an external source to an internal program memory after a reset signal is de-asserted. However, even if it were obvious to combine Baltz et al. with co-pending application 09/943,475, and Applicant maintains it is not, the combination would not result in double patenting.

The co-pending application claims a decompression of stored, compressed data by a decompression capability within the flash memory device. This type of decompression is not claimed in the present claims. Therefore, the claims of each application, even combined with cited art, are to two different inventions.

Claim Rejections Under 35 U.S.C. §102

Claims 1-3, 5, 11, 12, 15, 18 and 21 were rejected under 35 U.S.C. §102(e) as being anticipated by *Baltz et al.* (U.S. Patent No. 6,058,474). Applicant respectfully traverses this rejection.

Baltz et al. discloses a method for DMA boot loading for transferring a block of data from an external source to an internal program memory after a reset signal is de-asserted. However, *Baltz et al.* neither teaches nor suggests either a direct connection between the non-volatile memory device and the volatile memory device for direct transfer of data or the synchronous memory generating a system reset signal to the processor.

The Examiner states that the direct connection between the volatile memory device and the non-volatile memory device is indicated at column 7, lines 46 – 60 and the Abstract. However, these passages show a connection between a memory device and the microprocessor. There is no teaching or suggestion of a direct connection between a volatile memory and a non-volatile memory so that the processor does not need to get involved, as is claimed in the present application. The DMA process described in *Baltz et al.*, as is well known in the art and not described as being different therein, still requires intervention by the microprocessor and uses a system bus that is accessible by all components of the system.

The Examiner further states that signal 79 of *Baltz et al.* is the system reset signal that is generated by the volatile memory of the present invention. However, column 6, lines 43 – 45, column 7, lines 17 – 20, and Figure 4A & B clearly show that this signal is generated by the DMA controller in the CPU and not from any memory device.

Claim Rejections Under 35 U.S.C. §103

Claims 4, 6-9, 14, 16-19 were rejected under 35 U.S.C. §103(a) as being anticipated over *Baltz et al.* in view of *Harari et al.* (U.S. Patent No. 6,266,724). Applicant respectfully traverses this rejection.

All *Harari et al.* adds to the disclosure of *Baltz et al.* is a processor system that loads data from a flash memory over a serial connection. Since neither *Harari et al.* nor *Baltz et al.* teach or suggest Applicant's claimed invention, for the reasons discussed previously with respect to *Baltz et al.*, the combination of these references cannot render Applicant's invention obvious.

Claim 13 was rejected under 35 U.S.C. §103(a) as being anticipated over *Baltz et al.* in view of *Shin* (U.S. Patent No. 6,735,669). Applicant respectfully traverses this rejection.

For the above-described reasons, since claim 13 depends from a claim that Applicant believes is allowable, claim 13 would also be allowable. *Shin* does not add anything beyond a RAMBUS DRAM to the combination of the previously discussed references.

Claims 10 and 20 were rejected under 35 U.S.C. §103(a) as being anticipated over *Baltz et al.* in view of *Harari et al.*, as applied to claims 6 and 19 and further in view of *Shin*. Applicant respectfully traverses this rejection.

For the reasons that were discussed previously, neither *Baltz et al.*, *Harari et al.*, nor *Shin* individually or together, render the present claims obvious. None of these references teach or suggest Applicant's invention of a direct connection between a non-volatile memory device and a volatile memory device wherein the volatile memory generates a system reset signal to the processor to indicate successful completion of the data transfer.

CONCLUSION

For the above reasons, Applicant requests that the Examiner withdraw the rejections and allow the present claims. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2203. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

Date: 16 August 2004

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